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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/333,049	06/15/1999	HIROSHIGE HIRANO	0819-255	3672

7590 02/13/2002

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EXAMINER
PHAM, HOAI V

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/333,049	HIRANO ET AL.	
	Examiner	Art Unit	
	Hoai V Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations "an upper interlevel dielectric film formed to cover the first interconnection layer; a second interconnection layer formed on the upper interlevel dielectric film, wherein the second interconnection layer totally covers the top and bottom electrode of the ferroelectric capacitor in the plannar layout" in claims 8-9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Specification

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of 37 CFR 1.71(a)-(c):

> (a) The specification must include a written description of the invention or discovery and of the manner and process of making and using the same, and is required to be in such full, clear, concise, and exact terms as to enable any person skilled in the art or science to which the invention or discovery appertains, or with which it is most nearly connected, to make and use the same.
>
> (b) The specification must set forth the precise invention for which a patent is solicited, in such manner as to distinguish it from other inventions and from what is old. It must describe completely a specific embodiment of the process, machine, manufacture, composition of matter or improvement invented, and must explain the mode of operation or principle whenever applicable. The best mode contemplated by the inventor of carrying out his invention must be set forth.
>
> (c) In the case of an improvement, the specification must particularly point out the part or parts of the process, machine, manufacture, or composition of matter to which the improvement relates, and the description should be confined to the specific improvement and to such parts as necessarily cooperate with it or as may be necessary to a complete understanding or description of it.

The specification is objected to under 37 CFR 1.71 because the specification fails to provide an adequate written description the limitations in claims 8-9.

Claim Objections

3. Claims 1 and 6 are objected to because of the following informalities:

In claim 16, line 10, after "film" insert --;--.

In claim 6, line 7, change "a bit line" to --the bit line--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-7 and 8 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 1, line 13, the phrase "dummy bit lines connected to the ferroelectric capacitor" is not described in the specification. The dummy bit line is connected an associated doped layer (see specification, page 3, line 10).

In claim 8 recites the limitation "the upper interlevel" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-7, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (figs. 4-5, pages 2-3) in view of Chinu et al. [JP. 11121705 A] (applicant IDS) previously applied.

Applicant Admitted Prior Art discloses a ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode (58), a bottom electrode (56) and a ferroelectric film (57) interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layer (53) and a gate (54), the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film (59) formed over the memory cell transistor and the ferroelectric capacitor; and

a first interconnection layer (60) formed on the interlevel dielectric film;

a memory cell composed of the feroelectric capacitor and the memory cell transistor; and

dummy bit lines (DBL, /DBL) is arranged at the edge of the memory cell array, wherein the memory cell comprises a memory array arranged at the edge of the memory cell array.

Applicant Admitted Prior Art fails to show that wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode. However, Chinu et al. discloses that the first interconnection layer (73) formed on the interlevel dielectric film (71), wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer (73) partially overlaps with the top electrode (67a) of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line (B/L) formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode (see figures 6-7). Therefore, it would have been obvious to the skilled in the art to incorporate the teaching of Chinu et al. into the

Applicant Admitted Prior Art device in order to prevent coupling capacitance between the interconnection layer and top electrode or between the bit line and the top elecrode.

With respect to claims 2 and 6, Chinu et al. discloses a storage line (73) connected to the top electrode of the ferroelectric capacitor and to the first doped layer (57a) of the memory cell transistor, the storage line having a linear plannar pattern; and the bit line connected to the second doped layer of the memory cell transistor, and wherein the storage line intersects only one side of the top electrode in the planar layout.

With respect to claims 3 and 5, Chinu et al. discloses that a first region connectd to the top electrode of the ferroelectric capacitor; a second region connectd to the first doped layer (57a) of the memory cell transistor; and a third region being interposed between the first and second regions and intersecting the side of the top electrode in the planar layout, and wherein the line width of the third region is smaller than that of the first and second regions.

With respect to claim 4, Chinu et al. discloses that the bit line does not overlap with the top electrode in the planar layout.

With respect to claim 7, Chinu et al. discloses that the interconnection layer is containing at least one of aluminum and copper

8. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chinu et al. [JP. 11121705 A] (applicant IDS), previously applied, in view of Hayashi et al. [U.S. Pat. 6,174,766 B1] previously applied.

a ferroelectric capacitor including a top electrode (67a), a bottom electrode (63a) and a ferroelectric film (65a) interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layer (57a, 57b) and a gate (55), the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film (71) formed over the memory cell transistor and the ferroelectric capacitor; and

a first interconnection layer (73) formed on the interlevel dielectric film, wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer (73) partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode.

Chinu et al. does not disclose that an upper interlevel dielectric film formed to cover the first interconnection layer; a second interconnection layer formed on the upper interlevel dielectric film, wherein the second interconnection layer totally covers the top and bottom electrode of the ferroelectric capacitor in the plannar layout. However, Hayashi et al. shows that it is well known in the art to have an upper interlevel dielectric film (27) formed to cover the first interconnection layer (24, aluminum); and a second interconnection layer (30, aluminum) formed on the upper interlevel dielectric film, wherein the second interconnection layer totally covers the top and bottom electrodes of

the ferroelectric capacitor (see figure 13, col.13, lines 44+) in the cross-section view. Therefore, it would have been obvious to the skilled in the art to include the second interconnection layer in the Hayashi et al. for providing an electrical connection to other circuit.

Response to Arguments

9. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument that Hayashi is deficient in teaching , disclosing, or suggesting the positions of the second interconnection layer and the memoery cells in a planar layout as recited in claims 8 and 9. This argument is not persuasive since in the cross-section view of Hayashi, the second interconnection layer (30) formed on the upper interlevel dielectric film and covered both the top and bottom electrodes (14, 12) (see fig. 13). Therefore, the second interconnection layer (30) will be covered both the top and bottom electrodes in the planar layout. Furthermore, Applicants are submitting amended Figs. 1 and 3 with amendment shown in red ink to indicate the second interconnection layer. However, the red ink indicating the second interconnection layer is incorrect because these layers are cell plate lines which are the bottom electrode (16) (see page 9, lines 3-5 and page 13, lines 13-14). Also, the limitation "a second interconnection layer **totally covers** the top and bottom electrode " in claims 8 and 9 is not described in the specification. In the specification, the second

interconnection layer may cover the top or bottom electrode (see page 12, lines 24-25 to page13, line 1).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP
Hoai Pham
January 30, 2002

OLIK CHAUDHURI
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